1. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, each active pixel sensor having a respective internal offset voltage output superimposed on its respective active pixel sensor output, and wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, a method for canceling the internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said method comprising:

accessing a first row of said array to obtain a first sample of said given active pixel sensor output;

storing said first sample of said given active pixel sensor output of said first row of said array;

accessing a second row of said array, said first row of said array being the previous row to said second row of said array; and thereafter,

accessing said first row of said array a second time to obtain a second sample of said given active pixel sensor output;

storing said second sample of said given active pixel sensor output of said first row of said array; and

subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.

2. (Currently amended) A method in accordance with claim 1, said method comprising:

accessing a third row of said array, said first row of said array being a predetermined number of rows previous to said third row, whereby said method sets the image exposure time of said ~~semiconductor imaging chip~~ third row.

3. (Original) A method in accordance with claim 2, wherein said step of accessing said third row of said array occurs substantially simultaneously with said step of accessing said second row of said array.

4. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, a method for accessing the pixel signal values of said active pixel sensors, said method comprising:

accessing row N of said array a first time;

accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array; and thereafter

accessing row N of said array a second time.

5. (Original) A method in accordance with claim 4, wherein each active pixel sensor has a respective internal offset voltage output superimposed on its respective active pixel sensor output, and said method further includes canceling the respective internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said method further comprising:

storing a first sample of said given active pixel sensor of row N of said array during said first time;

storing a second sample of said given active pixel sensor of row of N of said array during said second time; and

subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.

6. (Currently amended) A method in accordance with claim 4, wherein said method further includes setting the image exposure time of said semiconductor imaging chip, said method comprising:

accessing row N+1+ M of said array, where M is a predetermined number of rows, whereby said method sets the image exposure time of said ~~semiconductor imaging chip~~third row.

7~~5~~. (Original) A method in accordance with claim 6, wherein said step of accessing said N+1+M row of said array occurs substantially simultaneously with said step of accessing said row N+1 of said array.

8~~6~~. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, a method for accessing the pixel signal values of said active pixel sensors, said method comprising:

accessing row N of said array a first time;

accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array;

accessing row N+1+ M of said array, where M is a predetermined number of rows; and

thereafter

accessing row N of said array a second time,

whereby said method sets the image exposure time of said ~~semiconductor imaging chip~~row N+1+M.

9~~.~~ (Original) A method in accordance with claim 8, wherein said step of accessing said N+1+M row of said array occurs substantially simultaneously with said step of accessing said row N+1 of said array.

10. (Original) A method in accordance with claim 8, wherein each active pixel sensor has a respective internal offset voltage output superimposed on its respective active pixel sensor output, and said method further includes canceling the respective internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said method further comprising:

storing a first sample of said given active pixel sensor of row N of said array during said first time;

storing a second sample of said given active pixel sensor of row of N of said array during said second time; and

subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.

11. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, each active pixel sensor having a respective internal offset voltage output superimposed on its respective active pixel sensor output, and wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, an apparatus for canceling the internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said apparatus comprising:

a first row driver coupled to a first row of said array to access said first row of said array to obtain a first sample of said given active pixel sensor output on a given column of said array;

a first memory element coupled to said given column, said first sample of said given active pixel sensor output of said first row of said array being stored in said first memory element;

a second row driver coupled to a second row of said array, said first row of said array being the previous row to said second row of said array to reset said given active pixel sensor;

a scan controller coupled to said first row driver to thereafter access said first row of said array a second time to obtain a second sample of said given active pixel sensor output on said given column of said array;

a second memory element coupled to said given column, said second sample of said given active pixel sensor output of said second row of said array being stored in said second memory element; and

a differential amplifier having first and second inputs, said first input of said differential amplifier coupled to said first memory element, said second input of said differential amplifier coupled to said second memory element, wherein said differential amplifier subtracts said second sample from said first sample to form said corrected output from said given active pixel sensor.

12. (Currently amended) An apparatus in accordance with claim 11, said apparatus comprising:

a third row driver coupled to a third row of said array to access said third row of said array, said first row of said array being a predetermined number of rows previous to said third row, whereby said apparatus sets the image exposure time of said ~~semiconductor imaging chip~~third row.

13. (Original) An apparatus in accordance with claim 12, wherein said scan controller coupled to said first, second and third row drivers causes said third row driver and said second row driver to access said array at substantially the same time.

14. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, an apparatus for accessing the pixel signal values of said active pixel sensors, said apparatus comprising:

a first row driver for accessing row N of said array a first time;

a second row driver for accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array; and

a scan controller coupled to said first row driver for thereafter accessing row N of said array a second time.

15. (Original) An apparatus in accordance with claim 14, wherein each active pixel sensor has a respective internal offset voltage output superimposed on its respective active pixel sensor output, and said apparatus further includes apparatus for canceling the

respective internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said apparatus further comprising:

a first memory element coupled to a given column of said array for storing a first sample of said given active pixel sensor of row N of said array during said first time;

a second memory element coupled to said given column for storing a second sample of said given active pixel sensor of row of N of said array during said second time; and

a differential amplifier having a first input coupled to said first memory element and a second input coupled to said second memory element for subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.

16. (Currently amended) An apparatus in accordance with claim 14, wherein said apparatus further includes apparatus for setting the image exposure time of said semiconductor imaging chip, said apparatus comprising:

a third row driver for accessing row N+1+ M of said array, where M is a predetermined number of rows, whereby said apparatus sets the image exposure time of said ~~semiconductor imaging chip~~third row.

17. (Original) An apparatus in accordance with claim 16, wherein said scan controller coupled to said first, second and third row drivers causes said third row driver and said second row driver to access said array at substantially the same time.

18. (Currently amended) In a semiconductor imaging chip having a plurality of active pixel sensors arranged in an array of rows and columns, wherein a current row of said array has an access line shared with a reset line of a previous row of said array to form a shared access/reset line which simultaneously accesses said current row and resets said previous row, an apparatus for accessing the pixel signal values of said active pixel sensors, said apparatus comprising:

a first row driver for accessing row N of said array a first time;

a second row driver for accessing row N+1 of said array, said row N of said array being the previous row to said row N+1 of said array;

a third row driver for accessing row N+1+ M of said array, where M is a predetermined number of rows; and

a scan controller coupled to said first row driver for thereafter accessing row N of said array a second time,

whereby said apparatus sets the image exposure time of said ~~semiconductor imaging chip~~row N+1+M.

19~~.~~. (Original) An apparatus in accordance with claim 18, wherein said scan controller coupled to said first, second and third row drivers causes said third row driver to access said N+1+M row of said array and said second row driver to access said N+1 row of said array at substantially the same time.

20. (Original) An apparatus in accordance with claim 18, wherein each active pixel sensor has a respective internal offset voltage output superimposed on its respective active pixel sensor output, and said apparatus further includes apparatus for canceling the respective internal offset voltage appearing at the output of a given active pixel sensor on said current row to form a corrected output, said apparatus further comprising:

a first memory element coupled to a given column of said array for storing a first sample of said given active pixel sensor of row N of said array during said first time;

a second memory element coupled to said given column for storing a second sample of said given active pixel sensor of row of N of said array during said second time; and

a differential amplifier having a first input coupled to said first memory element and a second input coupled to said second memory element for subtracting said second sample from said first sample to form said corrected output from said given active pixel sensor.